# SDD Review Document

## Summary

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| --- | --- |
| **Date** | 02/09/2021 |
| **Effort** | 1 hour |
| **Room/Location** | Viritual |
| **Review Status** | Open |
| **Review name** | SDD\_Template\_DIO.doc |
| **Method** | WT |
| **Release** | 1.0 |
| **Responsible** | Marco Antonio Mares Mejia |
| **Project** | Door Control Module |
| **Reason of Review** | Initial Release |

## Comment List/

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| --- | --- | --- | --- | --- | --- |
| **No.** | **Reference** | **Comments / Actions** | **Classification (E)rror/Risk / (R)emark** | **Responsible person/Planned date for completion** | **Completion(Name/Date)** |
| 1 | Header and/ Footer Page Information | No information is included in the Top Header and Bottom Footer of the pages. This is necessary in order to increasy document readibility. | Risk | Daniel Ramirez / 06/09/2021 |  |
| 2 | Functional Decomposition | DIO Component shall read values directly from the ECU. In ther SW Architecture, no relation between DIO and Signal Components are specified. Dio shall not receive nor report nothing to Signal Component | Error | Daniel Ramirez / 06/09/2021 |  |
| 3 | Activity Diagrams Improvement | In order to increase Activity Diagrams readability, is recommended to also include where the information is taken from using Object Flow Connectors. | Remark | Daniel Ramirez / 06/09/2021 |  |
| 4 |  |  |  |  |  |
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| 6 |  |  |  |  |  |
| … |  |  |  |  |  |

## Check List

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| --- | --- | --- | --- | --- | --- |
| No | Description | OK / NOK / NR | Comment | Responsible person /  Planned date for completion | Status |
| 1 | Does the design comply to the SW architecture? (interfaces, scheduling...) | NOK | A better analysis of the interfaces of DIO with other component shall be done in order to comply with the architecture. | Daniel Ramirez /  06/09/2021 | Open |
| 2 | Are all requirements allocated to Desing elements? | OK |  |  | Closed |
| 3 | Are all operations described in an adequate detail and with the adequate notation? | OK |  |  | Closed |
| 4 | Is the coupling level between SW parts (internal or externals) reduced to the minimum?  Is the justification of all global data written in the design document? | OK |  |  | Closed |
| 5 | Is each data owned by one unit?  If a data is public (for read and/or for write operations), is its access made using a method provided by the owner?  (if a method is provided for read and write operations on the same pubilc data, the data has to be private) | OK |  |  | Closed |
| 6 | How are the variables initialized? If not initialized, is the reason explained? | NR | Software Requirements document doesn’t include a specific initialization method. |  | Closed |
| 7 | Is the mechanism to initialise the functionality (when needed) described?  (eg: function calls, data acquisition …) | NR |  |  | Closed |
| 8 | In case of global variable (shared or not shared) used in reentrance function (reentrance raised by an ISR), is there a mechanism to avoid data modification during its treatment? | NR | No method is mentioned in SW Requirements. |  | Closed |
| 9 | Are Tasks, ISRs and event notification function kept as short as possible? | OK |  |  | Closed |
| 10 | Is the state variable only used in one single module?  (If the state variable needs to be visible from another module (to be avoided), indicate it in the design and use the mechanism of read copy on that variable). | OK |  |  | Closed |
| 11 | Is the event memorization (ex: flag) consumed at the end of each reccurence of a state machine?  Otherwise, the risk is to use an obsolete event (ex: event memorization consumption conditionned by a state transition). | NOK | Variable memorization is not described in any Function. |  | Open |
| 12 | In case of asynchronous reception of the same event by several objects (ex: state machine, C function called periodicly…), has each object its own memorization mechanism (ex: separate flags). | NR | This component mainly describes only one event. |  | Close |